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UTILITY PATENT APPLICATION TRANSMITTAL

Only for new nonprovisional applications under 37 CFR 1 53(b))

Attorney Docket No.	042390.P8842
First Inventor	Anne E. Miller
Title	COPPER POLISH SLURRY FOR REDUCED INTERLAYER...
Express Mail Label No.	EL034435678US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original and a duplicate for fee processing)
2. ☐ Applicant claims small entity status. See 37 CFR 1.27.
3. ☒ Specification [*Total Pages* 20]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (*if filed*)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. ☒ Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 8]
5. Oath or Declaration [*Total Pages* 6]
   a. ☐ Newly executed (original or copy)
   b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d))
   (for continuation/divisional with Box 18 completed)
   i. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1 63(d)(2) and 1 33(b)
6. ☐ Application Data Sheet. See 37 CFR 1.76
7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (*Appendix*)
8. Nucleotide and/or Amino Acid Sequence Submission
   (if applicable, all necessary)
   a. ☐ Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
   i. ☐ CD-ROM or CD-R (2 copies); or
   ii. ☐ paper
   c. ☐ Statements verifying identity of above copies

JC564 U.S. PTO 09/715690 11/16/00

ACCOMPANYING APPLICATION PARTS

9. ☐ Assignment Papers (cover sheet & document(s))
10. ☐ 37 C.F.R. § 3.73(b) Statement *(when there is an assignee)* ☒ Power of Attorney
11. ☐ English Translation Document *(if applicable)*
12. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
13. ☐ Preliminary Amendment
14. ☒ Return Receipt Postcard (MPEP 503)
    (Should be specifically itemized)
15. ☐ Certified Copy of Priority Document(s)
    (if foreign priority is claimed)
16. ☐ Request and Certification under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
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18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: ______

*Prior application Information: Examiner*______ *Group/Art Unit:* ______

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

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Signature	Donna Jo Coningsby	*Date*	11/16/00

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FEE TRANSMITTAL for FY 2000

Patent fees are subject to annual revision

TOTAL AMOUNT OF PAYMENT	($)	970.00

Complete if Known	
Application Number	
Filing Date	November 16, 2000
First Named Inventor	Anne E. Miller
Examiner Name	
Group/Art Unit	
Attorney Docket No.	042390.P8842

METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number: 02-2666

Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

☒ Charge Any Additional Fee(s) Required Under 37 CFR §§ 1 16, 1 17, 1.18 and 1 20

☐ Applicant claims small entity status. See 37 CFR 1 27.

2. ☒ Payment Enclosed:

☒ Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	710.00
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 710.00

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	30	- 20** =	10	X	18.00	=	$180.00
Independent Claims	4	- 3** =	1	X	80.00	=	$80.00
Multiple Dependent						=	

***or number previously paid, if greater, For Reissues, see below*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	260	204	135	Multiple Dependent claim, if not paid
109	80	209	40	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 260.00

FEE CALCULATION (continued)

3. ADDITIONAL FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	390	216	195	Extension for response within second month	
117	890	217	445	Extension for response within third month	
118	1,390	218	695	Extension for response within fourth month	
128	1,890	228	945	Extension for response within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	130	123	130	Petitions related to provisional applications	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b))	
179	710	126	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) ______________________

Other fee (specify) ______________________

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)

SUBMITTED BY

Complete (if applicable)

Name (Print/Type)	Donna Jo Coningsby	Registration No. (Attorney/Agent)	41,684	Telephone	(503) 684-6200
Signature	Donna Jo Coningsby			Date	11/16/00

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P8842 PATENT

COPPER POLISH SLURRY FOR REDUCED INTERLAYER DIELECTRIC EROSION AND METHOD OF USING SAME

Inventor: Anne E. Miller

"Express Mail" mailing label number EL034435678US

COPPER POLISH SLURRY FOR REDUCED INTERLAYER DIELECTRIC EROSION AND METHOD OF USING SAME

Inventor: Anne E. Miller

Background of the Invention

Field of the Invention

The invention relates generally to the manufacture of integrated circuits, and more particularly to slurries for use in chemical mechanical polishing of copper, copper alloys, and copper diffusion barriers in the formation of interconnect lines on integrated circuits.

Background

Advances in semiconductor manufacturing technology have led to the integration of tens, and more recently hundreds, of millions of circuit elements, such as transistors, on a single integrated circuit (IC). To achieve such dramatic increases in the density of circuit components has required semiconductor manufacturers to scale down the size of the circuit elements and the interconnection structures used to connect the circuit elements into functional circuitry, as well as scaling down the spacing between the interconnect.

Manufacturers of integrated circuits have recently shown great interest in replacing conventional aluminum and aluminum alloys with copper to form signal and power interconnections on integrated circuits. Copper interconnect lines have a number of advantages over conventional aluminum-based metallization schemes, including but not limited to, improved electromigration characteristics and lower resistivity per cross-sectional area. These are important attributes that make copper a preferred metallization scheme for manufacturers that continue to shrink the dimensions and line widths of the various elements that make up an integrated circuit.

Copper interconnect on integrated circuits is typically formed by way of a damascene process. This is in contradistinction to aluminum-based interconnections which are typically formed by way of the well-known subtractive etch process. As is known in this field, copper damascene processing involves defining an interconnection by forming trenches in a layer of insulating material having a planarized top surface, depositing a metal, such as copper, over the insulating material and into the trenches. If copper is the metal that is deposited, then a barrier layer that acts to reduce or eliminate the diffusion of copper into the insulating material is typically disposed over the insulating material prior to the deposition of the copper. The damascene process subsequently concludes with the removal of both the copper and barrier layer from the top surface of the insulating material, leaving the metal in the trenches such that these now represent individual interconnect lines.

The removal of the copper referred to above is typically achieved by way of chemical mechanical polishing. However, as the spacing between interconnect lines becomes very small, it has been observed that erosion of the insulating layer is greater in regions where interconnect density is greater. In other words, CMP with a conventional Cu polish has been observed to produce the aforementioned undesirable result of pattern sensitive erosion. This occurs even though many conventional slurries have a high selectivity to the barrier layer or a high selectivity to the oxide dielectric layer. This phenomenon is sometimes referred to as pattern sensitive erosion, the pattern density effect, the geometric effect, or similar expressions.

The non-uniform polishing that occurs due to the pattern density effect is undesirable because, among other things, it makes subsequent planarization operations more difficult, it makes the formation of trenches, and vias from upper interconnect levels more difficult, and it changes the designed for capacitance and resistance characteristics of the interconnect lines which in turns leads to compromised levels of performance and reliability.

What is needed are slurries and methods for polishing copper interconnects on integrated circuits that reduce the magnitude of pattern sensitive erosion of an interlayer dielectric material.

Brief Description of the Drawings

Fig. 1 is a schematic cross section of a portion of a wafer showing erosion of the ILD layer as a result of conventional CMP.

Fig. 2 is a bar graph showing the relative effectiveness of various surfactants on reducing pattern sensitive erosion.

Fig. 3 is a bar graph showing the relative removal rates of Cu and ILD using slurries with and without a surfactant additive.

Fig. 4 is a scatter graph showing Cu removal rate and static etch rate as a function of the concentrations of benzotriazole and cetyltrimethylammonium bromide.

Fig. 5 is a schematic cross section of a wafer showing the improvement in pattern sensitive erosion with a surfactant additive in the slurry.

Fig. 6 is a flow diagram of a process of polishing copper in accordance with the present invention.

Fig. 7 is a flow diagram of a process of making copper interconnect on integrated circuits in accordance with the present invention.

Fig. 8 is a flow diagram of a process of making a slurry in accordance with the present invention.

Fig. 9 is a flow diagram of a process of making a slurry in accordance with the present invention.

Detailed Description

<u>Overview</u>

Copper interconnect lines on integrated circuits are typically formed by damascene metallization processing which includes removal of excess copper

and copper barrier layers by way of CMP. When CMP is performed with conventional slurries, pattern sensitive erosion is observed in areas of the integrated circuit having high interconnect density. Fig. 1 illustrates the problem of increased levels of erosion in the high density interconnect areas. As shown in Fig. 1, an interlayer dielectric (ILD) **102**, has trenches lined with a copper diffusion barrier **104**, and further has copper metal **106** overlying the diffusion barriers **104**, and essentially filling the trenches. A polishing pad **110**, together with a plurality of slurry particles **108** are shown to illustrate the polishing process which produces erosion **112**. Pattern sensitive erosion produces greater levels of erosion in areas where the ratio of metal to dielectric is high, than in areas of the integrated circuit where interconnect lines are relatively sparse, and therefore the width of the interlayer dielectric, i.e., the space between interconnect lines is greater.

One approach to solving this problem for integrated circuits which use Ta as the Cu diffusion barrier involves a two-step polishing process and the use of slurry having a high selectivity to Ta. However, the thickness of the barrier layer is not sufficient to protect the dense structure from erosion. It is also desirable to polish the copper and barrier layer as a one-step operation. Attempts to solve either of these problems by simply creating a slurry with a high ILD selectivity (e.g., <10 angstroms per min SiO_2 removal rate) have not improved dishing or erosion issues.

Embodiments of the present invention achieve the desired performance improvement for copper polishing by providing a slurry that includes a surfactant. The slurry in accordance with the present invention is used to remove excess Cu and Cu diffusion barrier while substantially reducing pattern sensitive erosion of the ILD. Embodiments of the present invention include a surfactant in the slurry that interacts sufficiently to improve the pattern density effect.

Slurries for use in the chemical mechanical polishing (CMP) of copper and copper diffusion barriers that reduce pattern sensitive erosion of an underlying

dielectric layer in accordance with the present invention, include at least one surfactant. Inclusion of surfactants, such as cetyltrimethylammonium bromide in a slurry mixture can reduce pattern sensitive erosion of dielectric materials such as silicon oxide, and fluorinated oxides of silicon that would otherwise occur during CMP of copper and copper diffusion barriers as is typical in the formation of copper interconnect lines in integrated circuits.

Referring to Fig. 2, a bar graph is provided that indicates the pattern density effect improvements, and the barrier selectivity improvements that result from the use of various surfactant additives. The first five additives shown in Fig. 2 are non-ionic surfactants, the sixth additive is an anionic surfactant, the seventh additive is an amphoteric surfactant, and the last three additives are cationic tertiary amine salts. Detailed chemical formulations are given in Table 1. In the experiments from which this data is obtained, the patterned erosion rate is measured on an SiOF patterned wafer based on a 3mm x 3mm structure with 6 micron wide metal lines, a spacing between the metal lines of 0.8 microns, and an etch depth of 6,000 angstroms. The base slurry without additive has a nearly zero (i.e., <10 angstroms per minute) blanket SiOF polish rate. This would correspond to a Cu:SiOF selectivity of > 200

Methods for forming copper based interconnect lines on integrated circuits in accordance with the present invention are described herein which include various polishing parameter ranges such as, for example, polishing pressures, spindle rpm, wafer rpm, slurry flow rates, delta P, and the use of a new class of slurry formulations.

<u>Terminology</u>

The terms, chip, integrated circuit, monolithic device, semiconductor device, and microelectronic device, are often used interchangeably in this field. The present invention is applicable to all of the above as they are generally understood in the field.

The expression, low dielectric constant material, refers to materials having a lower dielectric constant than silicon dioxide. For example, organic polymers, amorphous fluorinated carbons, nanofoams, silicon based insulators containing organic polymers, fluorine doped oxides of silicon, and carbon doped oxides of silicon have lower dielectric constants than silicon dioxide.

Erosion, as used herein, refers to the amount of a layer, typically an interlayer dielectric, that is removed during the polishing of a metal damascene structure. Erosion is measured as a thickness, or distance, and more particularly, it is a measure of the distance between the original surface of the layer and its post-polish surface. Erosion is generally an undesirable overpolishing. Examples of erosion can be seen in Fig. 1. Typically, the erosion, or interlayer dielectric loss, is greater for structures such as serpentines, and other patterns of high interconnect density, where the metal density is high relative to that of the dielectric, than it is for other areas of an integrated circuit having a relatively lower density of metal interconnect lines.

The letter k, is often used to refer to dielectric constant. Similarly, the terms high-k, and low-k, are used in this field to refer to high dielectric constant and low dielectric constant respectively, where high means greater than the dielectric constant of silicon dioxide, and low means lower than the dielectric constant of silicon dioxide.

Reference herein to “one embodiment”, “an embodiment”, or similar formulations, means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of such phrases or formulations herein are not necessarily all referring to the same embodiment. Furthermore, various particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

Slurry

A first exemplary formulation (Slurry Formulation #1) of a slurry in accordance with the present invention includes, per liter of final slurry, a surfactant such as 0.25 wt% cetyltrimethylammonium bromide, a chelating buffer system, such as 2.57 g/l citric acid and 3.66 g/l potassium citrate, an abrasive, such as 1.1 vol% 5 nm silica (surface area = 500 m^2/g), an oxidizer, such as 3.2 wt% hydrogen peroxide, and a corrosion inhibitor, such as 0.085 M/l benzotriazole. Such a slurry formulation has a pH of 3.8, and a slurry density of 1.03 g/ml.

The chelating buffer system may also be described as a combination of a chelating agent and a buffering agent. The chelator and the buffer may be either the same or different constituents.

Various changes in the formulation of a slurry in accordance with the present invention may be made. Such slurries contain a surfactant of a type and concentration that reduces or eliminates pattern-sensitive erosion. For example, a surfactant such as cetyltrimethylammonium bromide from 0.0001 M to 0.1 M may be used. A preferred range for cetyltrimethylammonium bromide is from 0.003 M to 0.075 M. Alternatively, cetyltrimethylammonium hydroxide may be used as the surfactant. In a further alternative embodiment, cetyltrimethylammonium bromide and cetyltrimethylammonium hydroxide are both used in the slurry of the present invention. The hydroxide, and hydroxide/bromide combination appear to give better results in terms of corrosion. Whereas the cetyltrmethylammonium cation controls the pattern sensitive erosion. An abrasive, such as SiO_2 from 0.25 to 10 vol.% may be used. A preferred range of SiO_2 abrasive is 0.50 to 2 vol.%. A chelating agent such as citric acid/potassium citrate, or ammonium bicitrate/potassium citrate may be used where the total citric acid plus citric acid salt concentration is between 0.02 M and 0.1 M inclusive. A buffer such as citric acid/potassium citrate may be used, where the total citric acid plus citric acid salt concentration is between 0.02

M and 0.1 M inclusive. A corrosion inhibitor such as benzotriazole may be used in a range of concentrations from 0.001 M to 0.05 M. Similarly, a corrosion inhibitor such as cetyltrimethylammonium bromide may be used in a range of concentrations from 0.001 M to 0.1 M, and preferably in the range of 0.003 M to 0.075 M.

In alternative embodiments of the present invention, the surfactant chosen to be combined into the slurry mixture may be a cation surfactant such as, for example, a quaternary ammonium halide, or a quaternary ammonium hydroxide; or a nonionic surfactant such as, for example, a dimethyl silicone ethylene oxide, or an alkyl polyethylene oxide. Furthermore, the surfactant may be dodecyltrimethylammonium chloride, dodecyltrimethylammonium bromide, cetyltrimethylammonium chloride, octadecylmethylpolyoxyethyleneammonium chloride, or an alkyltrimethylammonium halide wherein the alkyl group has more than twelve carbons.

A slurry in accordance with the present invention generally has a pH in the range of 3 to 6, and a density in the range of 1.02 to 1.05.

<u>Process</u>

In the following descriptions, it will be recognized by those skilled in this field that the numerical values of the various parameters are to be read with conventionally understood accuracies and therefore the illustrative embodiments are not meant to be unnecessarily limited.

In one embodiment, copper is polished with a slurry (such as, for example, Slurry Formulation #1, described above), under the following conditions: an IPEC 576 Orbital Polisher (from Speed-Fam IPEC, 305 North 54th Street, Chandler, AZ 85226), pressure of 2 psi, spindle rpm of 440, wafer rpm of 27, slurry flow rate of 100ccm, delta P of -0.4 psi, a IC1000 pad, and a suba4 subpad (from Rodel, 3804 East Watkins Street, Phoenix, AZ 85034). On blank test wafers the following the results were obtained: a copper removal rate of

2130 angstroms per minute, an SiOF ILD removal rate of <10 angstroms per minute, a static etch rate of 8 angstroms per minute, a Ta barrier layer removal rate of 20 angstroms per minute and a TaN barrier layer removal rate of 41 angstroms per minute. In a 90% dense structure the following results are obtained: 431 angstroms per minute erosion rate.

Referring to Fig. 3, an example of the reduction of the rate of pattern sensitive erosion with the use of a slurry in accordance with the present invention is shown. Fig. 3 is a bar graph and shows a first bar **302** representing the removal rate of blanket copper. This is the polish rate measured at pressure of 2 psi, spindle rpm of 440, wafer rpm of 27, slurry flow rate of 100ccm, delta P of -0.4 psi, a IC1000 pad, and a suba4 using a slurry without a surfactant, and a second bar **304** representing the ILD erosion rate in regions having 90% interconnect density using the same slurry. Fig. 3 also shows third bar **306** representing the removal rate of blanket copper using a slurry with a surfactant in accordance with the present invention, and a fourth bar **308** representing the ILD erosion rate in regions having 90% interconnect density using the same slurry. From the bar graph of Fig. 3, it can be seen that although there is a slight decrease in copper removal rate when chemical mechanical polishing is performed with the slurry of the present invention, there is a substantial decrease in the undesired pattern sensitive erosion rate of the ILD. Additionally, there is only a negligible difference between the removal rates of blanket SiOF ILD when using slurries with and without the surfactant in accordance with the present invention. This indicates that methods which address the removal rates of blanket ILD material may not be suitable for solving the problem of pattern sensitive ILD erosion.

Referring to Fig. 4, the effect of benzotriazole and cetyltrimethylammonium bromide on polish rate and static etch rate are shown. As shown in Fig. 4, with the addition of cetyltrimethylammonium bromide, a

reduction in static etch rate is achieved, thereby indicating that the concentration of benzotriazole could be reduced to enhance the copper etch rate.

In accordance with the present invention, the magnitude of pattern sensitive erosion of the ILD during the removal of copper and a copper barrier layer is reduced by addition of, at least, one surfactant to the slurry. Referring to Fig. 5, an interlayer dielectric (ILD) **102**, has trenches lined with a copper diffusion barrier **104**, and further has copper metal **106** overlying the diffusion barriers **104**, and essentially filling the trenches. A polishing pad **110**, together with a plurality of slurry particles **108** are shown to illustrate the polishing process. Also shown in Fig. 5, are schematic representations of the surfactant additives **202** that are useful in reducing pattern sensitive erosion. As can be seen in Fig. 5, pattern sensitive erosion **212** is substantially reduced over what is produced in the prior art process of polishing copper. The surfactant combined with the slurry mixture is characterized by an ability to substantially prevent abrasive particles in the slurry from removing an oxide dielectric while allowing the removal of copper and tantalum-based copper diffusion barriers. ILD **102** may be a doped or undoped oxide of silicon. Various dopants such as, but not limited to, fluorine are often added to oxides of silicon in order to reduce the dielectric constant of the ILD. Although Figure 5 shows the surfactant attaching to the ILD, it is understood that the surfactant may also attach to the abrasive particles depending on the particle surface chemistry.

Referring to Fig. 6, a flow diagram of a method of polishing copper in accordance with the present invention is described. Those skilled in this field are familiar with the process of forming copper interconnect on integrated circuits. Cu interconnect lines and associated vias, are formed in accordance with a damascene metallization process. For example, a barrier layer and seed layer are deposited over the patterned ILD top surfaces including the trench and via openings. Cu is then plated and the excess copper is removed by a chemical mechanical polishing (CMP) process that includes the use of a slurry. The

expression copper damascene structure may be used to describe the patterned ILD with copper diffusion barriers disposed between the ILD and an overlying layer of copper. At block **602** a wafer having a copper damascene structure thereon is brought into contact with a polishing pad. In an illustrative example of the present invention, an IC1000 pad with a suba4 subpad is used on an IPEC 576 Orbital Polisher. At block **604** a CMP operation is performed by polishing the copper damascene structure of the wafer with a polishing pad (described above) and a slurry including a surfactant that reduces the ILD removal rate to a greater extent than the copper removal rate. An example of such a surfactant is cetyltrimethylammonium bromide. As is well-known in the field of chemical mechanical polishing, the slurry is typically dispensed onto the polishing pad. Slurries may be pre-mixed and pumped to the dispensing outlet, or various ingredients of the slurry may be dispensed onto the polishing pad to form the final slurry at that point.

Fig. 7 is a flow diagram of an illustrative embodiment of the present invention in which copper interconnect lines are formed. At block **702** trenches are formed in a planarized low-k dielectric layer by conventional patterning methods. Fluorinated silicon oxide (SiOF) is an example of a low-k dielectric. At block **704** the surfaces of the patterned low-k dielectric layer are covered, that is lined, with a copper diffusion barrier. Tantalum-based, i.e., tantalum or tantalum nitride, barrier layers are commonly used as copper diffusion barriers in integrated circuits. At block **706** a layer of copper is formed over the diffusion barrier. At block **708** excess copper is removed by chemical mechanical polishing with a slurry containing an additive that reduces pattern sensitive erosion.

Referring to Fig. 8 an exemplary process for forming a slurry in accordance with the present invention is described. At block **802** a mixture is created by combining an abrasive and an oxidizer with water. At block **804** a surfactant is added to the mixture, the surfactant being characterized in that it

reduces ILD removal rate without significantly affecting copper removal rate when chemically mechanically polishing copper with the mixture. Those skilled in the art and having the benefit of this disclosure will recognize that the specific order and rates of adding the various ingredients to the mixture may be varied without departing from the nature of the invention.

Referring to Fig. 9, a exemplary process of making a slurry in accordance with the present invention is described. At block **902** a mixture is created by combining silica, hydrogen peroxide, and cetyltrimethylammonium bromide. At block **904** a chelating agent is combined with the mixture. Potassium citrate is an example of a chelating agent that may be used in the present invention. At block **906** a buffering agent is combined with the mixture. Potassium citrate/citric acid is an example of a buffering chemistry that may be used in the present invention. At block **908** a corrosion inhibitor is combined with the mixture. Benzotriazole is an example of a corrosion inhibitor that may be used with the present invention.

It will be understood that the ingredients used to prepare a slurry in accordance with the present invention may be combined in different sequences. For example, water and benzotriazole may be combined, then buffers and chelating agents added, followed, respectively, by the addition of cetyltrimethylammonium bromide, silica, and hydrogen peroxide.

<u>Conclusion</u>

Embodiments of the present invention are useful at least for manufacturing integrated circuits and provide a slurry for chemical mechanical polishing of copper wherein the slurry contains an additive to reduce the geometric, or pattern-density effect on the ILD polish rate.

An advantage of some embodiments of the present invention is that integrated circuits with closely spaced damascene interconnects can be formed without significant ILD erosion.

Whenever copper is referred to herein, it should be understood that the present invention is applicable to various alloys of copper.

It will be understood that various other changes in the details, materials, and arrangements of the parts and operations which have been described and illustrated herein may be made by those skilled in the art without departing from the principles and scope of the invention as expressed in the subjoined Claims.

What is claimed is:

1. A slurry, comprising a mixture of:

a surfactant; a chelating buffer system; an abrasive; an oxidizer; and a corrosion inhibitor.

2. The slurry of Claim 1, wherein the surfactant comprises cetyltrimethylammonium bromide dissolved in the mixture.

3. The slurry of Claim 1, wherein the surfactant comprises cetyltrimethylammonium cations and halogen anions.

4. The slurry of Claim 3, wherein the abrasive comprises silica, the corrosion inhibitor comprises benzotriazole, and the oxidizer comprises hydrogen peroxide dissolved in the mixture.

5. The slurry of Claim 1, wherein the chelating buffer system comprises ammonium bicitrate and potassium citrate dissolved in the mixture.

6. The slurry of Claim 1, wherein the chelating buffer system is selected from the group consisting of citric acid/potassium citrate, and ammonium bicitrate/potassium citrate.

7. The slurry of Claim 1, wherein the corrosion inhibitor is selected from the group consisting of benzotriazole and cetyltrimethylammonium bromide.

8. The slurry of Claim 1, wherein the surfactant comprises between 0.003M and 0.075M cetyltrimethylammonium bromide in the mixture.

9. The slurry of Claim 1, wherein the surfactant comprises cetyltrimethylammonium hydroxide dissolved in the mixture.

10. The slurry of Claim 1, wherein the surfactant comprises both cetyltrimethylammonium hydroxide and cetyltrimethylammonium bromide dissolved in the mixture.

11. A copper polish slurry, comprising in combination:

water, a surfactant, a chelating buffer system, an abrasive, a oxidizer, and a corrosion inhibitor.

12. The method of Claim 11, wherein the abrasive comprises silica having a surface area 500 m^2/g.

13. The method of Claim 12, wherein the corrosion inhibitor is selected from the group consisting of benzotriazole and cetyltrimethylammonium bromide.

14. The method of Claim 11, wherein the corrosion inhibitor is benzotriazole and the surfactant is selected from the group consisting of cetyltrimethylammonium bromide and cetyltrimethylammonium hydroxide.

15. The method of Claim 14, wherein the slurry has a pH of 3.8 and a density of 1.03 g/ml.

16. The method of Claim 15, wherein the oxidizer comprises hydrogen peroxide; and the chelating buffer system comprises citric acid and potassium citrate.

17. A method of making a slurry for the chemical mechanical polishing of copper and copper diffusion barriers, comprising:

combining a surfactant; a chelating buffer system; an abrasive; an oxidizer; and a corrosion inhibitor.

18. The method of Claim 17, wherein the surfactant comprises cetyltrimethylammonium bromide and cetyltrimethylammonium hydroxide.

19. The method of Claim 17, wherein the surfactant comprises a quaternary ammonium halide.

20. The method of Claim 17, wherein the surfactant comprises a dimethyl silicone ethylene oxide.

21. The method of Claim 17, wherein the surfactant comprises an alkyl polyethylene oxide.

22. The method of Claim 17, wherein the surfactant comprises a material characterized by an ability to substantially prevent abrasive particles in the slurry from removing a oxide dielectric while allowing the removal of copper and tantalum-based copper diffusion barriers.

23. The method of Claim 22, wherein, the oxide dielectric is doped so as to have a dielectric constant less than that of silicon dioxide.

24. The method of Claim 18, wherein, the oxide dielectric is doped with fluorine.

25. A method of polishing copper, comprising:

bringing a substrate coated on at least one surface with copper, into contact with a polishing pad; and

dispensing onto the polishing pad, a slurry formed from a combination of an abrasive, an oxidizer, and a surfactant.

26. The method of Claim 25, wherein the surfactant is selected from the group consisting of quaternary ammonium halide, dimethyl silicone ethylene oxide, and alkyl polyethylene oxide.

27. The method of Claim 25, wherein the surfactant comprises cetyltrimethylammonium bromide.

28. The method of Claim 25, wherein the surfactant is characterized by an ability to substantially prevent abrasive particles in the slurry from removing a oxide dielectric while allowing the removal of copper and tantalum-based copper diffusion barriers.

29. The method of Claim 27, wherein a concentration of cetyltrimethylammonium bromide in the slurry is in the range of 0.003M to 0.075M.

30. The method of Claim 25, wherein the surfactant comprises cetyltrimethylammonium hydroxide.

ABSTRACT OF THE DISCLOSURE

Slurries for use in the chemical mechanical polishing (CMP) of copper and copper diffusion barriers that reduce pattern sensitive erosion of an underlying dielectric layer include at least one surfactant. Inclusion of surfactants, such as cetyltrimethylammonium bromide in a slurry mixture can reduce pattern sensitive erosion of dielectric materials such as silicon oxide, and fluorinated oxides of silicon that would otherwise occur during CMP of copper and copper diffusion barriers as is typical in the formation of copper interconnect lines in integrated circuits.

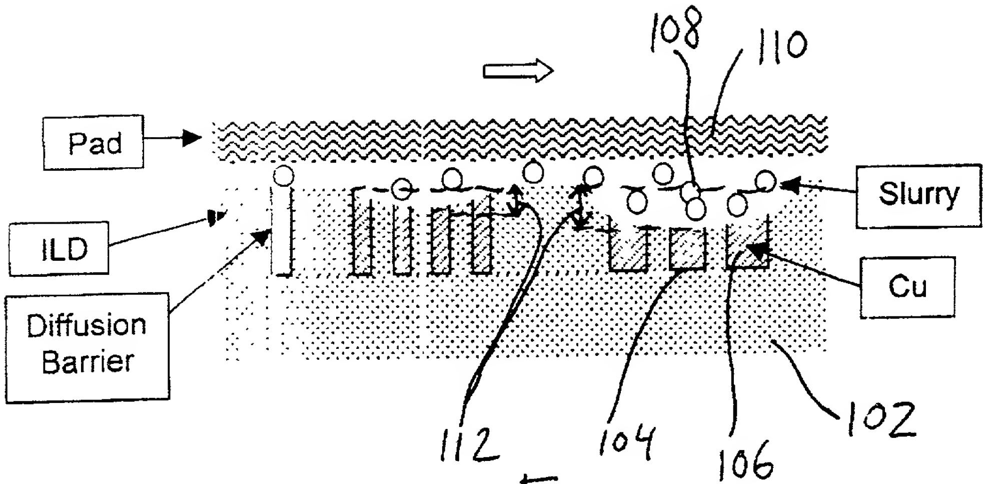
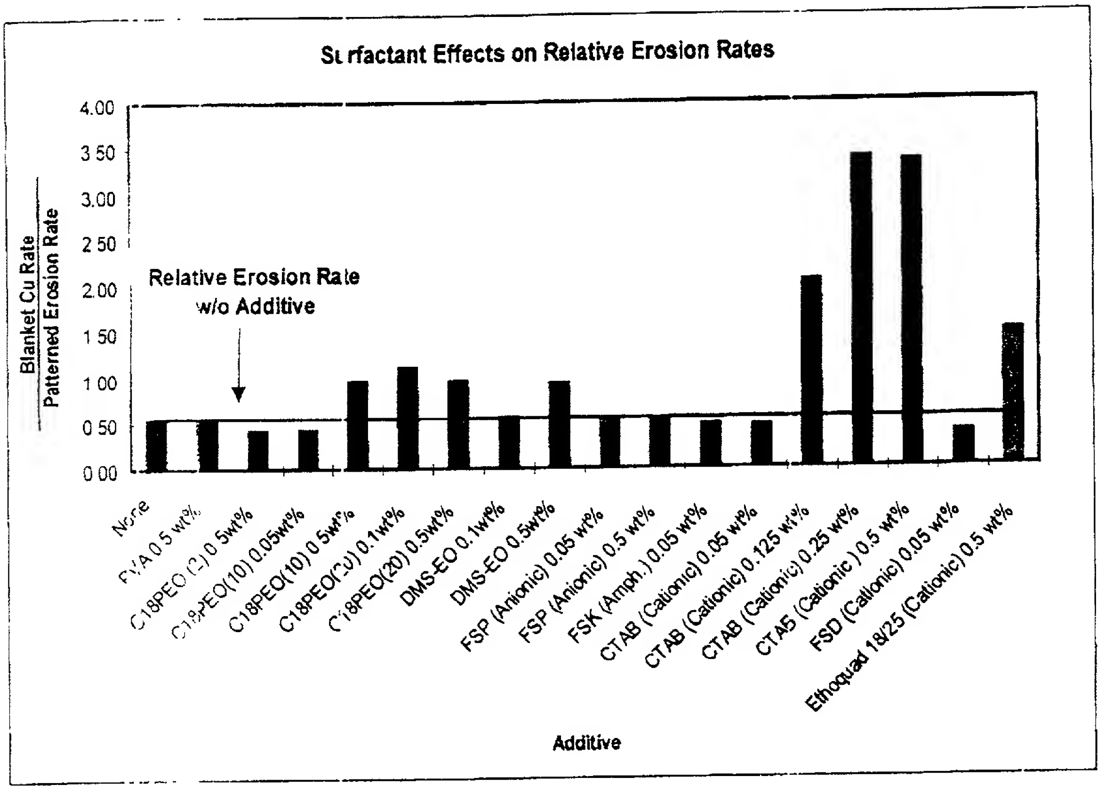
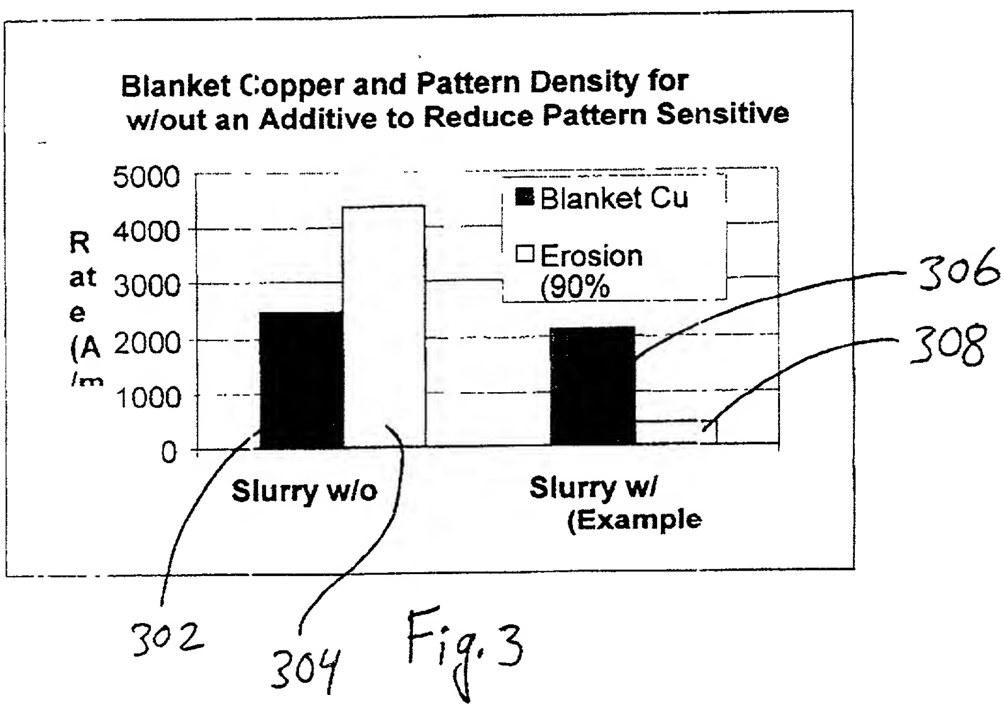


Fig. 1



Surfactant Effects on Relative Erosion Rates
Blanket Cu Rate
Patterned Erosion Rate
4.00
3.50
3.00
2.50
2.00
1.50
1.00
0.50
0.00
Relative Erosion Rate
w/o Additive
None
PVA 0.5 wt%
C18PEO(2) 0.5wt%
C18PEO(10) 0.05wt%
C18PEO(10) 0.5wt%
C18PEO(20) 0.1wt%
C18PEO(20) 0.5wt%
DMS-EO 0.1wt%
DMS-EO 0.5wt%
FSP (Anionic) 0.05 wt%
FSP (Anionic) 0.5 wt%
FSK (Amph.) 0.05 wt%
CTAB (Cationic) 0.05 wt%
CTAB (Cationic) 0.125 wt%
CTAB (Cationic) 0.25 wt%
CTA5 (Cationic) 0.5 wt%
FSD (Cationic) 0.05 wt%
Ethoquad 18/25 (Cationic) 0.5 wt%
Additive

Fig. 2



Blanket Copper and Pattern Density for
w/out an Additive to Reduce Pattern Sensitive
5000
4000
3000
2000
1000
0
Rate (A/m
Blanket Cu
Erosion (90%
Slurry w/o
Slurry w/ (Example
306
308
302
304

Fig. 3

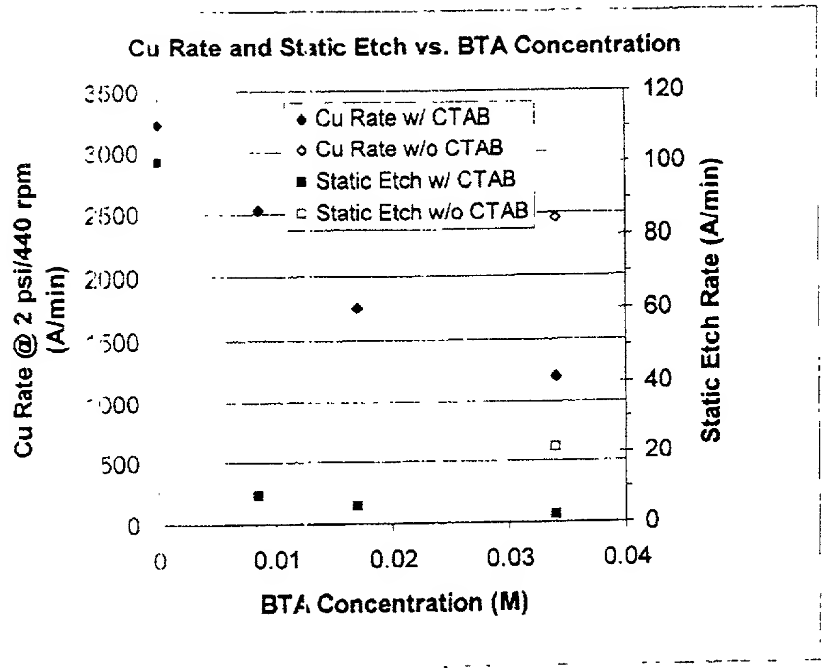

Cu Rate and Static Etch vs. BTA Concentration
Cu Rate w/ CTAB
Cu Rate w/o CTAB
Static Etch w/ CTAB
Static Etch w/o CTAB
Cu Rate @ 2 psi/440 rpm (A/min)
Static Etch Rate (A/min)
BTA Concentration (M)
0
500
2000
2500
3000
3500
0.01
0.02
0.03
0.04
20
40
60
80
100
120

Fig. 4

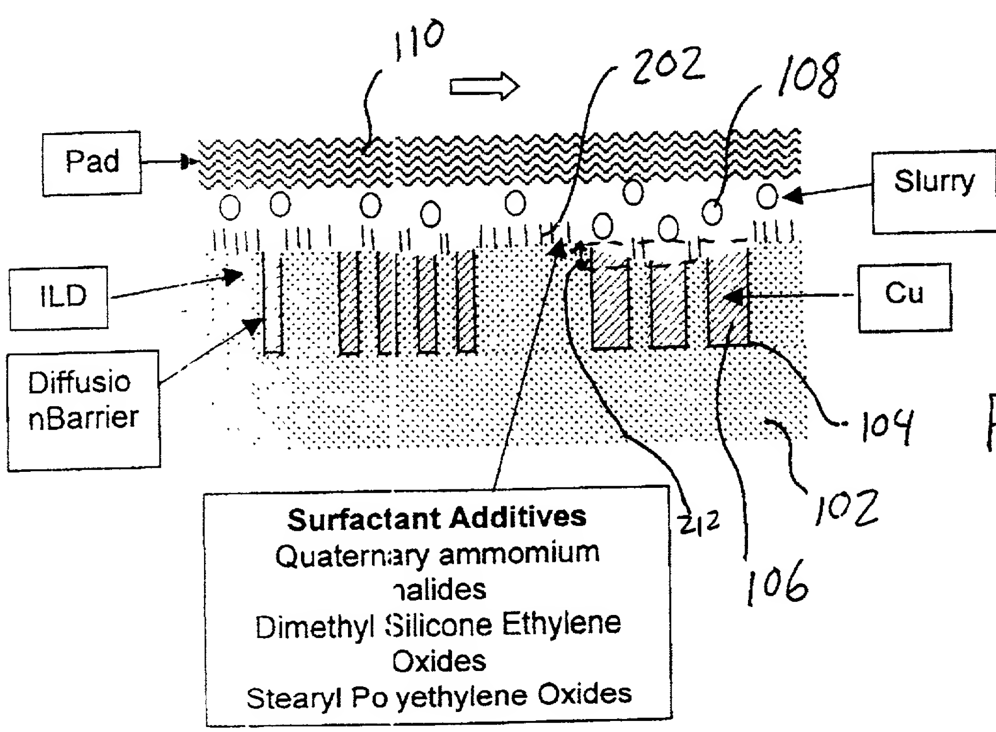

110
202
108
Pad
Slurry
ILD
Cu
Diffusio nBarrier
104
102
212
106
Surfactant Additives
Quaternary ammomium
halides
Dimethyl Silicone Ethylene
Oxides
Stearyl Po yethylene Oxides

Fig. 5

602

Bring a wafer having a copper damascene structure thereon into contact with a polishing pad

604

Perform CMP on the copper damascene structure with a slurry including a surfactant that reduces the ILD removal rate to a greater extent than the copper removal rate

Fig. 6

702

Form trenches in a planarized low-k dielectric layer

704

Line surfaces of the low-k dielectric layer with a copper diffusion barrier

706

Form a layer of copper over the diffusion barrier

708

Perform CMP with a slurry containing an additive that reduces pattern sensitive erosion

Fig. 7

802

Create a mixture by combining an abrasive and an oxidizer with water

804

Add a surfactant to the mixture, the surfactant being characterized in that it reduces ILD removal rate without significantly affecting copper removal rate when chemically mechanically polishing copper with the mixture

Fig. 8

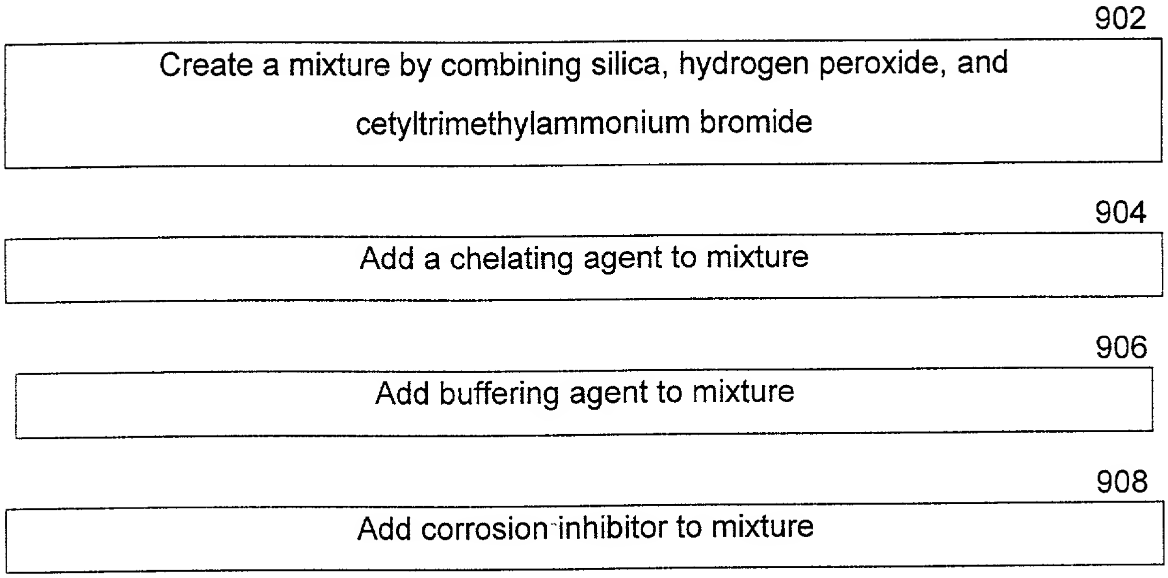

902
Create a mixture by combining silica, hydrogen peroxide, and cetyltrimethylammonium bromide
904
Add a chelating agent to mixture
906
Add buffering agent to mixture
908
Add corrosion inhibitor to mixture

Fig. 9

Table 1

Abreviation	Name	Chemical Formula	Surfactant Type	ILD Interaction Site
PVA 0.5 wt%	Polyvinylalchohol	$[-CH_2CH(OH)-]_n$ (MW = 85,000-146,000)	nonionic	Si-O-Si, OH
C18PEO (2)	Polyoxyethlene(2)stearylether	$C_{18}H_{37}(OCH_2CH_2)_2OH$	nonionic	Si-O-Si, OH
C18PEO(10)	Polyoxyethlene(10)stearylether	$C_{18}H_{37}(OCH_2CH_2)_{10}OH$	nonionic	Si-O-Si, OH
C18PEO(20)	Polyoxyethlene(20)stearylether	$C_{18}H_{37}(OCH_2CH_2)_{20}OH$	nonionic	Si-O-Si, OH
DMS-EO	Ethylene oxide modified	$Me_3SiO(Me_2SiO)[(CH_2)(OCH_2CH_2)_nOMe](MeSiO)SiMe_3)$*	nonionic	Si-O-Si, OH
FSP	Phosphate fluorosurfactant	$[F(CF_2CF_2)_zCH_2CH_2O]_xP(O)(ONH_4)_y$	anionic	$SiOH_2^+$
FSK	Amphoteric Flurosurfactant	$F(CF_2CF_2)_yCH_2CHO(Ac)CH_2N^+(CH_3)_2CH_2COO^-$	amphoteric	SiO^-, $SiOH_2^+$
CTAB	Cetyltrimethylammonium bromide	$C_{16}H_{33}N(CH_3)_3Br$	cationic	SiO^-
FSD	Quaternary Ammonium	$F(CF_2CF_2)_y alkyl N^+R_3Cl^-$ (Proprietary)	cationic	SiO^-
Ethoquad 18/25	Octadecylmethylpolyoxyethylene(15)ammonium	$RN(CH_3)[(CH_2CH_2O)_{\sim 7.5}H][(CH_2CH_2O)_{\sim 7.5}H]Cl$	cationic	SiO^-
K-Oleate 0.5	Potassium Oleate	$CH_3(CH_2)_7CH=CH(CH_2)_7CO_2K$	anionic	$SiOH_2^+$

*Me=CH_3 R=Hydrocarbon group alkyl = Alkyl group

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

COPPER POLISH SLURRY FOR REDUCED INTERLAYER DIELECTRIC EROSION AND METHOD OF USING SAME

the specification of which

[X] is attached hereto.
[ ] was filed on ______________ as
United States Application Number ______________
or PCT International Application Number ______________
and was amended on ______________.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, **month**, year)	PRIORITY CLAIMED UNDER 37 USC 119
			[ ] No [ ] Yes
			[ ] No [ ] Yes
			[ ] No [ ] Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to:
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(Name of Attorney or Agent)
12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to:
Raymond J. Werner, (503) 684-6200.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Residence ______________________ Citizenship ____________
(City, State) (Country)

P. O. Address ______________________________

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(City , State) *(Country)*

P. O. Address ______________________

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Inventor's Signature ______________________ Date ______________

Residence ______________________ Citizenship ______________

(City , State) *(Country)*

P. O. Address ______________________

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Inventor's Signature ______________________ Date ______________________

Residence ______________________ Citizenship ______________________

(City, State) *(Country)*

P. O. Address ______________________

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Full Name of Eleventh/Joint Inventor (given name, family name) ______________________

Inventor's Signature ______________________ Date ______________________

Residence ______________________ Citizenship ______________________

(City, State) *(Country)*

P. O. Address ______________________

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